AMENDMENT TO THE SPECIFICATION

Please replace the title of the application with the following replacement title:

GENERATION OF INTERLEAVED PARITY CODE WORDS
HAVING LIMITED RUNNING DIGITAL SUM VALUES

After the paragraph that appears on page 5, lines 1-3 of the specification, that begins with "FIG. 5 is a flow chart...", please insert the following eleven new paragraphs that read as follows:

FIG. 6 is a block diagram of another embodiment of a system for encoding and transmitting data according to the present invention.

FIG. 7 is a flow chart depicting a system for encoding and transmitting data according to the present invention, according to an illustrative embodiment.

FIG. 8 is a flow chart depicting a system for encoding and transmitting data according to the present invention, according to another illustrative embodiment.

FIG. 9 is a flow chart depicting a system for encoding and transmitting data according to the present invention, according to another illustrative embodiment.

FIG. 10 is a flow chart depicting a system for encoding and transmitting data according to the present invention, according to another illustrative embodiment.

FIG. 11 is a flow chart depicting a system for encoding and transmitting data according to the present invention, according to another illustrative embodiment.

FIG. 12 is a flow chart depicting a system for encoding and transmitting data according to the present invention, according to another illustrative embodiment.

FIG. 13 is a flow chart depicting a system for encoding and transmitting data according to the present invention, according to another illustrative embodiment.

FIG. 14 is a flow chart depicting a system for encoding and transmitting data according to the present invention, according to another illustrative embodiment.

FIG. 15 is a flow chart depicting a system for encoding and transmitting data according to the present invention, according to another illustrative embodiment.

FIG. 16 is a flow chart depicting a system for encoding and transmitting data according to the present invention, according to another illustrative embodiment.

Please replace the paragraph that appears on page 18, line 11 through page 19, line 3 of the specification, that begins with "The RLL encoder 162..." with the following replacement paragraph:

Parity of greater than modulus 2 is also possible, and will be desirable for some applications due to an enhanced capability for error correction. In one illustrative embodiment depicted in FIG. 11, analogous in many steps to FIG. 5, illustrative method 1100 includes illustrative optional condition 1119, associated generally with steps 1118, 1120, and 1122, wherein a parity encoder adapted to generate a second interleaved parity code word incorporating information from the first DCF code word, and to provide the second interleaved parity code word to a channel. For instance, if two parity bits are added and the base is calculated with a simple counting code, where each bit may contribute either 1 or 0 to the base, then a modulus of 3 is defined. No matter what input code word is presented, the parity encoder can produce a corresponding parity code word congruent to either 0, 1 or 2 modulo 3. Similarly, greater error correction may be provided by using a greater number of parity bits above 2. The running digital sum of a code word may also serve as the base of the code word.

Please replace the paragraph that appears on page 18, line 11 through page 19, line 3 of the specification, that begins with "The RLL encoder 162..." with the following replacement paragraph:

The RLL encoder 162 is adapted to receive the data to be encoded, in the form of data sequences, and to generate an RLL code word of r bits as output corresponding to an input data sequence. The RLL encoder 162 adds at least one bit to an input data sequence to generate a

corresponding RLL code word having a run length limit k, where the run length limit is the maximum number of zeroes in a row contained within the RLL code word. A typical value of k might be from 6 to 10, but could be consistent with providing a signal at any integer from 1 through 100, depending on the needs of the particular application in which the embodiment is used. For example, a value k=4 would provide for particularly high assurance of the reliable performance of a phase lock oscillator (PLO), while a value of k=100 would provide an extraordinarily advantageous code rate while still providing the advantage of an RLL condition, for applications without substantial PLO sensitivity. An illustrative example of this is depicted in FIG. 16, wherein method 1600 is an embodiment that includes step 1602, optional condition 1604, and step 1606, wherein optional condition 1604 includes wherein the RLL encoder is adapted such that the RLL code word has a run length limit k that is an integer from the range of 4 through 100. Method 1600 is otherwise similar to FIG. 5, described below. Other embodiments with values of k even lower than 4 and higher than 100 would be appropriate for other conditions.

Please replace the paragraph that appears on page 22, lines 6-19 of the specification, that begins with "The result of the concatenating encoding..." with the following replacement paragraph:

The result of the concatenated encoding is to provide an overall write code word, as an interleaved parity code word in this embodiment, to the channel. The system may also comprise a decoder 152 adapted to receive the write code word, in particular the interleaved parity code word, from the channel 150, as depicted for example in FIG. 6. The decoder is adapted to decode the code word in light of the encoding used by the particular embodiment, and generate therefrom a read signal. The read signal will consist of the same or a substantially similar sequence of bits as the original input data sequence, particularly as ensured by the various error correction methods apparent in the encoding as discussed above.

Please insert, on page 23, line 19 of the specification, immediately after the paragraph that appears on page 23, lines 9-18 that begins with "The bits are only reordered...," the following new paragraph:

FIG. 12 depicts illustrative method 1200, according to an illustrative embodiment analogous in many steps to FIG. 5. Method 1200 includes illustrative optional condition 1219, associated generally with steps 1218, 1220, and 1222, to generate a second interleaved parity code word incorporating information from the first DCF code word, and provide the second interleaved parity code word to a channel.

Please insert, on page 24, line 24 of the specification, immediately after the paragraph that appears on page 24, lines 12-23 that begins with "For example, in an embodiment conforming again to FIG. 2," the following new paragraph:

Other illustrative options for the values of n and the maximum absolute value of the DCF code words are depicted in FIGS. 7 through 10 as step 730, which includes different illustrative optional conditions in each of FIGS. 7 through 10. Step 730 follows steps 210 and 212 and is followed by step 738, in a method otherwise analogous to that of method 200 of FIG. 5, in each of FIGS. 7 through 10. In FIG. 7, step 730 of method 700 includes the illustrative optional conditions 732 and 734. In FIG. 8, step 730 of method 800 includes the illustrative optional conditions 732 and 834. In FIG. 9, step 730 of method 900 includes the illustrative optional conditions 732, 934 and 936. In FIG. 10, step 730 of method 1000 includes the illustrative optional conditions 732, 934 and 1036.

Please insert, on page 26, line 13 of the specification, immediately after the paragraph that appears on page 26, lines 1-12 that begins with "At step 214, the data word...," the following three new paragraphs:

FIGS. 13 through 15 depict additional illustrative embodiments of encoding system methods. FIG. 13 depicts method 1300 according to an illustrative embodiment, which is analogous to method 200 except as depicted otherwise. Method 1300 includes additional step 1331, and optional conditions 1333 and 1335, associated with steps 1318, 1320 and 1322. Step 1331 includes to generate a first parity code word and a second parity code word, and interleave the first parity code word and the second parity code word. Condition 1333 includes that d is a modulus, and the first parity code word comprises receiving a first code word that incorporates information from the first DCF code word, and adding d-1 parity bits to the first input code word. Condition 1335 includes that generating the second parity code word comprises receiving a second input code word, and adding d-1 parity bits to the second input code word. Condition 1335 may have one of two further conditions, 1337 and 1339, associated with it. Condition 1337 includes that the second input code word also incorporates information from the first DCF code word. Condition 1339 includes that the second input code word incorporates information from the second DCF code word.

FIG. 14 depicts method 1400, according to an illustrative embodiment which is analogous to method 1300 except as depicted otherwise. Method 1400 includes additional step 1331 and optional condition 1333, and associated with steps 1418, 1420 and 1422. Optional condition 1333 may have either of additional optional conditions 1435 and 1437 associated with it, and condition 1437 may further have optional condition 1439 associated with it. Optional condition 1435 includes that generating the second parity code word comprises receiving a second input code word, and adding d-1 parity bits to the second input code word. Optional condition 1437 includes that generating the first parity code word further comprises selected a first residue r1, wherein the d-1 parity bits added to the first input code word are such that a base of the first parity code word is congruent to r1 modulo d. Optional condition 1439 includes that the base of the first parity code word is the digital sum of the first input code word.

FIG. 15 depicts method 1500, according to an illustrative embodiment which is analogous to method 1300 except as depicted otherwise. Method 1500 includes additional step 1531, associated with steps 1518, 1520 and 1522, step 1531 including to generate a first parity code word and a second parity code word, and interleave the first parity code word and the

second parity code word. Step 1531 may also include either of optional conditions 1535 or 1537, in different embodiments. Condition 1535 includes such that generating the first interleaved parity code word comprises re-ordering bits of the first parity code word and of the second parity code word according to a pseudorandom rule. Condition 1537 includes such that generating the first interleaved parity code word comprises re-ordering bits of the first parity code word and of the second parity code word according to a bit-wise rule.